

REMARKS

Claims 1-30 as originally filed, including independent claims 1, 11 and 21, were pending in the subject application prior to the amendments set forth above. New claim 31 is added by the amendments set forth above, such that after entry of said amendments, claims 1-31 will be pending, including independent claims 1, 11 and 21.

Amendments

No new matter is added by the current amendments. Support for new claim 31 and for the amendments to claim 1 may be found, for example, in paragraph 33 of the subject application, page 10 lines 4-18, together with Figure 6A. An example of the "first symbol set representing a transmitted data set encoded by a first constituent coding process" is X_k , $Y0_k$ and $Y1_k$, and an example of the "distinct second symbol set representing the transmitted data set encoded by a second constituent coding process" is X_k , $Y0'_k$ and $Y1'_k$. These symbol sets are generally well understood in the art, but exemplary details of the coding process that creates these symbol sets in the transmitter, as well as exemplary details of decoding and de-interleaving in prior art receivers, are described in the parent application of which the subject application is a continuation-in-part (U.S. patent application 09/668,059 entitled "Turbo Decoding" filed September 20, 2000, "the parent application"), on page 1 line 29 - page 3 line 7, with reference to Figures 1 and 2 of the parent application.

An exemplary process for decoding and de-interleaving such symbols (X , $Y0/Y0'$, $Y1/Y1'$) is described in the subject application in paragraphs 34-36, page 10 line 20 - page 12 line 8, with reference to Figures 6A and 7. As described, decoding is performed by the same APP decoder engine 146 of Figure 6A for each of the two constituent codes. In the example of Figure 7, the first constituent code symbols RSC1 are decoded (steps 171-175) for a complete frame (step 176) before the second constituent code symbols RSC2 are decoded (steps 177-181). Each decoding step employs feedback (such as in Figure 6A from MUX 162 to INPUT BUFFER 144), except that such information is not "feedback" during the first half of the first iteration, as no output has yet been derived from a symbol set representing the transmitted data set. However, subsequent iterations will use feedback for decoding from symbols of both constituent codes. Symbols from each constituent code are conveyed on the same lines, as may be seen by the input lines from channel de-interleaver 142 to input buffer 144 which show $Y0$ and $Y0'$ sharing a line, as well as $Y1$ and $Y1'$ sharing another line. The conveyance is nonconcurrent, as may be seen, for example, from the steps 173 and 179 of Figure 7.

The sections of the specification identified above also support the current amendments to claims 11 and 21 that clarify the meaning of "storing received data and decoded data in a single common buffer, the common buffer sized to hold a single frame of received data." Properly construed in light of the specification, (de)-interleaver buffer 150 (Figure 6A) is an example of the "common buffer." As may be seen from steps 175, 181 and 184 of Figure 7 (describing operation of the apparatus shown in Figure 6A), the same interleaver buffer 150 stores each output from the decoder engine 146, including the interim estimates (*i.e.*, partially decoded symbols based on constituent code symbols that have been processed at least once by the decoder) from each constituent code. The final current amendments to claims 11 and 21 are supported in the specification at page 12, lines 5-8, in respect of the exemplary apparatus of Figure 6A.

The following remarks explain the current amendments to claims 1, 11 and 21 for the record, as may be required for later determining whether the claim has been "narrowed for reasons of patentability" in view of the *Festo* line of cases, and does not express an argument or disagreement with the Examiner. In each of these claims, the descriptive phrase "a single" was intended to convey a limitation to "a single," or in other words "only a single" of the item thus described. As an example, in claim 1 as originally filed, the phrase a "single constituent code decoder" was intended to distinguish from plural decoders, such as 84 and 96 of Figure 5B. Paragraph 32 of the subject application describes the apparatus 140 illustrated in Figure 6A as including "a single APP decoder engine 146" (page 9 lines 29-30), and also points out that "the [single] APP decoder engine 146 functions as the first and second A Posteriori Probability ("APP") decoder[s] 84 and 96 of Figure 5B." Thus, the term "a single" decoder was meant to convey a distinction over two (or more) decoders. The current amendment of claim 1 clarifies that the same single decoder decodes both constituent codes. Without reference to the specification, it would otherwise be possible to construe "a single decoder" to mean nothing more limiting than "a decoder," such that the claim would appear to read on an apparatus including one, two or more decoders. Properly construed in view of the specification, it may be seen that claim 1 as presently amended is clarified, but not narrowed, as compared to claim 1 as originally filed. To reduce possible ambiguity, the meaning of "constituent code" is also clarified in claim 1 consistent with the specification.

Similarly as remarked on above with respect to claim 1, claims 11 and 21, as originally filed, conveyed a limiting meaning by the description "a single" item, whether a single frame of data, or a single buffer. Construed literally without careful reference to the specification, the phrase may appear non-limiting. By the current amendment, claims 11 and 21 are accordingly clarified to reflect the "only one" sense of the phrase that is conveyed by the context of the application. Clarification in respect of "[data] stored in a single buffer" includes first clarifying that the relevant data is that which is partially decoded (*i.e.*, has been processed at least once through the decoder engine 146 in Figure 6A), and requiring that "all" such data is thus stored; otherwise, it might appear that another buffer could be required to hold part of such data, and the

claimed single buffer would therefore not be "single" as intended. A "single frame of data" is similarly clarified, both by elaborating "frame of data" to avoid potential ambiguities, and to convey the properly limiting sense of "a single." Accordingly, as currently amended in this regard, claims 11 and 21 both recite in part (new wording underlined): "storing all received data of the frame that is partially decoded data in a single common buffer, the common buffer required to hold only one block of data, each representing a soft estimate of one bit, for each bit encoded in the single frame of received data." All of these amendments thus clarify the amended claims as filed such that the literal construction is more precisely in line with the proper construction of the claims as filed that is conveyed in careful view of the specification. As such, the amendments are clarifying, rather than narrowing.

Rejections Under 35 USC 102

In section 1.1 of the current Office Action, the Examiner rejects claims 1-30 as anticipated by Haller et al. ("Haller"). The Examiner points out that the memory structure of Haller is suggested (col. 6 lines 16 *et seq.*) for use in interleaving and/or de-interleaving packet data in a cellular telephone.

Though describing the use of single port memories, which are also preferred for use in apparatus described in the subject application, Haller fails to teach, suggest or disclose features required by each of independent claims 1, 11 and 21, as currently amended.

Claim 1 as presently amended, for example, is distinguished by its requirement of a single constituent code decoder that is configured to derive estimates from both first and second constituent coded symbols. Haller suggests that the single-port memory may be "utilized as a memory bank within an interleaver control which manages the interleaving and/or de-interleaving of packet data transferred in a communication system, such as a cellular telephone system," but makes no suggestion whatsoever in regard to a decoder. As such, Haller does not (and cannot) suggest the requirements for the decoder that are recited in claim 1 as currently amended, and accordingly cannot anticipate claim 1 as currently amended.

Claims 11 and 21, as presently amended, each require in part (underlining added for emphasis):

storing all received data of the frame that is partially decoded data in a single common buffer, the common buffer required to hold only one block of data, each representing a soft estimate of one bit, for each bit encoded in the single frame of received data.

While it is true that a preferred embodiment of the invention employs single-port memories that have similarities to those described in Haller, claims 11 and 21 require very specific use of memory. Indeed, claims 11 and 21 do not even require that the memory be single-port. As remarked above in regard to claim 1, Haller merely suggests utilizing (the single-port) memory as "a memory bank" for interleaving and/or de-

interleaving packet data. There is no suggestion that the memory should be used as "a single common buffer" storing "all received data ...", as is required by claims 11 and 21.

Even more significantly, Haller makes no suggestion about the quantity of data that such singular buffer should be required to hold. Utilizing memory for interleaving and/or de-interleaving has been required since turbo decoding was first invented. Haller makes the further suggestion that single-port memory be utilized for this purpose, but otherwise adds nothing to the state of the art of memory utilization for symbol decoding/de-interleaving.

The Applicant, by contrast, describes steps and apparatus by which the memory required for decoding/de-interleaving may be substantially reduced (indeed, halved) compared to the prior art (as illustrated in Figure 5B). A design properly satisfying the limitations of claims 11 and 21 in accordance with the teaching of the specification can achieve such reduction of memory, thereby significantly reducing the amount of integrated circuit that is required for this task. Of course, the Applicant cannot, and does not, claim "reducing memory," but rather claims specific features that may result in such benefits. The benefits that can accrue are not claimed, but provide meaning and importance to the features that are claimed.

Haller fails to teach, disclose or fairly suggest any of the limitations of claims 11 and 21, as currently amended, which are set forth above and underlined. As such, Haller cannot anticipate either of claims 11 and claim 21, as currently amended. Accordingly, Haller does not anticipate any of the Applicant's independent claims 1, 11 and 21, as currently amended, and therefore also fails to anticipate any other pending claim in the subject application, at least because each properly depends from one of the independent claims 1, 11 and 21.

Rejections Under 35 USC 112

In section 3.1 of the current Office Action, the Examiner rejects claims 1, 11 and 21 under 35 USC 112 for lacking a de-interleaving limitation.

The rejected claims 1, 11 and 21, as currently amended, each suggest in the preamble that the defined invention is for "decoding and de-interleaving a received signal." As the Applicant more narrowly defines the invention in dependent claims, specific limitations on de-interleaving are required in dependent claims 2, 3, 8, 12, 13, 18, 22, 23 and 28. In its broadest embodiments, however, the Applicant requires no specific limitation in respect of de-interleaving.

De-interleaving is not necessary unless one wishes to practice the invention as suggested by the preamble, *i.e.*, for decoding and de-interleaving received data. To employ the invention thus, however, requires no limitations that are not well-known in the prior art. At least some suitable methods and apparatus for de-interleaving are well known in the prior art. Limitations that are well-known in the prior art need not be explicitly set forth in the body of the claim: being well known, such limitations are, by definition, not

inventive, and not being inventive, they do not form part of "the subject matter which the applicant regards as his invention."

Accordingly, the Examiner is respectfully requested to withdraw this ground of rejection.

Rejections Under 35 USC 101

In section 4.1 of the current Office Action, the Examiner rejects claims 21-30 as claiming non-statutory subject matter. More specifically, the Examiner seems to suggest that the claims are directed to an article of manufacture wherein codes are to be transmitted on a network. The Examiner references the last line of the specification.

This ground of rejection may be based on a misunderstanding. The article of manufacture defined according to claim 21, as presently amended, comprises "computer readable storage media including program logic embedded therein." No requirement for transmitting the program logic of such article of manufacture over a network is set forth in any of claims 21-30, as presently pending.

The claimed article of manufacture is defined by the steps that the embedded control logic causes control circuitry to perform. The last few lines of the Applicant's specification merely suggest a variety of possible ways that such an article of manufacture can cause control circuitry to perform as required. The Examiner seems to object to one such possible way of causing the required performance: namely, transmitting the code on a network from the article of manufacture to remotely-located control circuitry. However, "network" is a very broad term, and remote control of circuitry is well known. As such, a skilled person should be able to implement an embodiment of the invention defined by claim 21 to cause remote circuitry to perform as required by conveying (transmitting) appropriate code, stored in the claimed article of manufacture, to such remote circuitry.

While such implementation might not be useful, other suggested implementations are clearly useful and constitute statutory subject matter (e.g., firmware in a semiconductor memory, as would typically be included with a cellular telephone mobile station). It is respectfully submitted that the existence of a possible embodiment that may not be useful does not, *ipso facto*, render an invention contrary to 35 USC 101. In view of the existence of embodiments that clearly satisfy the requirements of 35 USC 101, the Examiner is respectfully requested to withdraw this ground of rejection, or to kindly explain in more detail how the disclosure of an additional possible embodiment can render the subject matter of a claim non-statutory.

Conclusion

The remarks set forth above address each ground of rejection set forth by the Examiner in the current Office Action. The remarks demonstrate clearly that each of the pending independent claims, as pending after

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entry of the amendment set forth above, is properly allowable over the cited prior art. The remarks also are believed to overcome the Examiner's rejections under 35 USC 112 and 35 USC 101. The Examiner is therefore respectfully requested to reconsider the application and to promptly issue a Notice of Allowance of all pending claims.

The Commissioner is authorized to construe this paper as including a petition to extend the period for response by the number of months necessary to make this paper timely filed. Fees or deficiencies required to cause the response to be complete and timely filed may be charged, and any overpayments should be credited, to our Deposit Account No. **50-0490**.

Respectfully submitted,

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